
2010 - A YEAR IN REVIEW
SEMATECH
POWERING COLLABORATIVE INNOVATION

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Message from Dan Armbrust

This has been a remarkable year for SEMATECH, and for our industry. In addition to preparing for the game-changing transitions on the horizon—in areas such as 3D interconnects, EUV lithography, and the 450 mm wafer transition—we are also exploring a host of novel options in materials and device structures. These advances, taken together, will drive and sustain our industry's technology roadmap and keep the industry on its historic productivity curve over the next decade.

As we embrace these new opportunities, there are challenges to overcome—the technical challenges of meeting increasingly complex performance, power, functionality and cost requirements, and the business challenges of creating new markets, making significant investments, and growing revenues in a dynamic economic environment.

Of course, each organization needs to determine its own positioning in the market, and its own business and technology strategies to address these challenges, but it is clear that no one can go it alone in the semiconductor business these days. It might have been possible once, in a vertically integrated company that did everything in-house—systems, design, chip technology, assembly and packaging, and maybe even building tools—but no longer. Consolidation and increasing segmentation have changed the landscape of our industry's structure and major players, as companies are becoming more divergent and specialized. As we explore multiple technology options and contend with rising R&D and manufacturing costs, it is more important than ever that we share resources, cost, and risk. So we are finding that even as companies differentiate from one another, they are interdependent and networked with one another as never before, to enable wise technology and investment decisions.

Certainly this is a positive trend. We know that our collective success as an industry depends on comprehensive industry-wide collaboration to reduce costs. The challenges of new technology introduction and profitable manufacturing are global, and cut across industry sectors; integrated device makers, foundries, and design, fabless/fablite, packaging/assembly, equipment, and materials companies all have a stake in solving them, as do the universities, research institutes, consortia, and governments that enable and support our industry. Increasingly we are working together across the industry ecosystem—through consortia and alliances—to integrate roadmaps, share the R&D and manufacturing investment burden, and cultivate new sources of leveraged funding.

As a member-driven global consortium, SEMATECH's role is to align roadmaps, R&D, and financial investments on behalf of our members, partners, and the industry. With a focus on both early development and manufacturability, we drive technical consensus, pull research into the industry mainstream, and lead major programs to address critical industry transitions. It's a powerful mission and model. Over our 22-year history, we have evolved with a dynamic industry, proven the success of public-private partnerships, and been the catalyst for both technology commercialization and economic development.

Together with our strategic partner, the University at Albany's College of Nanoscale Science and Engineering (CNSE), SEMATECH continued in 2010 to expand our coordination and oversight of next generation research, development, and commercialization progr ams in areas such as lithography, 3D interconnects, front end processes, and metrology—while extending our global reach and influence through program partnerships around the world in emerging semiconductor and nanotechnology driven applications. Our collaboration with CNSE, as an early partner and as one of the growing number of high-tech companies engaged at the Albany NanoTech Complex, is a platform for our ongoing cooperative research and development programs, enabling our program expansion and paying real dividends in cutting-edge research.

In 2010, as you will read in our annual review, we made significant technology and manufacturing advances, launched several major initiatives, and diversified our membership. We refined our strategy and redoubled our efforts to bring the industry together and build the common infrastructure and standards for major transitions in lithography, interconnects, materials and device structures, and manufacturing. To understand and represent the needs of the entire industry value chain and address critical infrastructure gaps, SEMATECH continued to create new cross-disciplinary engagements, including the following:

- Mature Technology Fabs program—reaching out to companies with "mature" or mainstream fabs, and providing a tailored set of councils and forums aimed at their specific productivity and cost challenges
- 3D Enablement program—launching a new 3D program with SIA and SRC to meet the standards and infrastructure needs of diverse constituencies (high performance, mobile, analog, mixed signal, MEMS, fabless, fablite, IDMs)
- Fabless program—bringing the design/fabless and technology/manufacturing communities together to share knowledge and roadmaps, and close infrastructure gaps
- EMI (EUV Mask Infrastructure) program—connecting multiple segments of the EUV supply chain in a partnership to collectively fund the development of key metrology tools by equipment suppliers
- Program memberships—partnering with a growing number of equipment and materials manufacturers in relevant portions of our advanced technology and manufacturing programs

These new collaborations and other major initiatives in the planning stages represent new opportunities for our members and the industry at large to engage in relevant collaborative R&D.

We are proud of our accomplishments in 2010, and look forward to even greater opportunities and accomplishments in the years ahead. Together with our members and partners, SEMATECH is paving the way for our industry's continued success in technology innovation and manufacturing productivity.

Dan Armbrust

President and CEO, SEMATECH

Vision

SEMATECH is the world's catalyst for fostering pre-competitive cooperation across the nanoelectronics industry and accelerating the commercialization of technology innovations into manufacturing solutions. By setting global direction, creating opportunities for flexible collaboration, and conducting strategic R&D, SEMATECH and its subsidiaries deliver significant return on investment to our semiconductor and emerging technology partners.

The Power of Collaboration

Setting New Directions for Our Industry

Semiconductors are a foundational technology, ubiquitous in a whole range of consumer and business products, and an epochal innovation that drives our economy and is indispensable to our everyday lives.

Particularly in the semiconductor industry, it is critical to deliver the right product to market at the right time and within budget. The dual challenges of meeting the growing demand for technological innovation and increasing consumer expectations for more sophisticated products at ever-lower prices impose significant pressures on the industry.

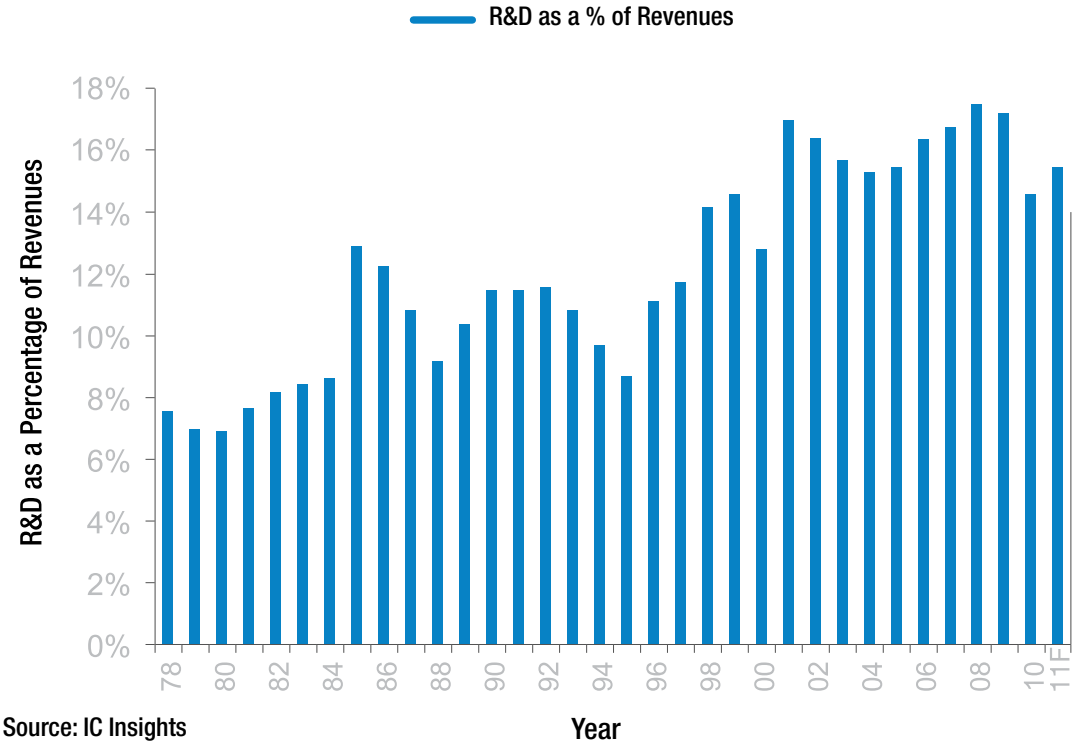
One area under pressure is industrial research. In a race against the *International Technology Roadmap for Semiconductors* (ITRS), companies must decrease time to market for new innovations and conduct research aimed at specific, identifiable customer needs. These pressures are compounded by two-year product development cycles in which companies refresh their product lines every 18–24 months. Costs and capital expenditures are escalating, influenced by increasingly complex research pipelines and extreme market cycles. In fact, in 2010 industry invested over $130 billion in research and development, a 32.5 percent increase from 2009.

Since the 1980's, SEMATECH has played a pivotal role in alleviating industry pressures by effectively managing cross-industry pre-competitive collaborative efforts. At SEMATECH we bring chipmakers and other industry sectors together to share costs and risk and to solve common technical and manufacturing challenges. Our network of value-driven programs helps our members develop solutions to the industry's most pressing challenges—solutions that lead to many of the industry's technological breakthroughs.

In addition to lowering R&D costs, SEMATECH is helping semiconductor manufacturers achieve innovative technology solutions, improve manufacturing productivity, mitigate risks and reduce time to market.

Pre-competitive collaboration is an effective way to adapt to the constantly changing realities of the semiconductor market and is essential in the quest for technology solutions, best practices, cost-effective manufacturing, optimal use of scarce research dollars and diverse external sources of R&D funding.

Worldwide Semiconductor R&D Spending Trends



Source: IC Insights

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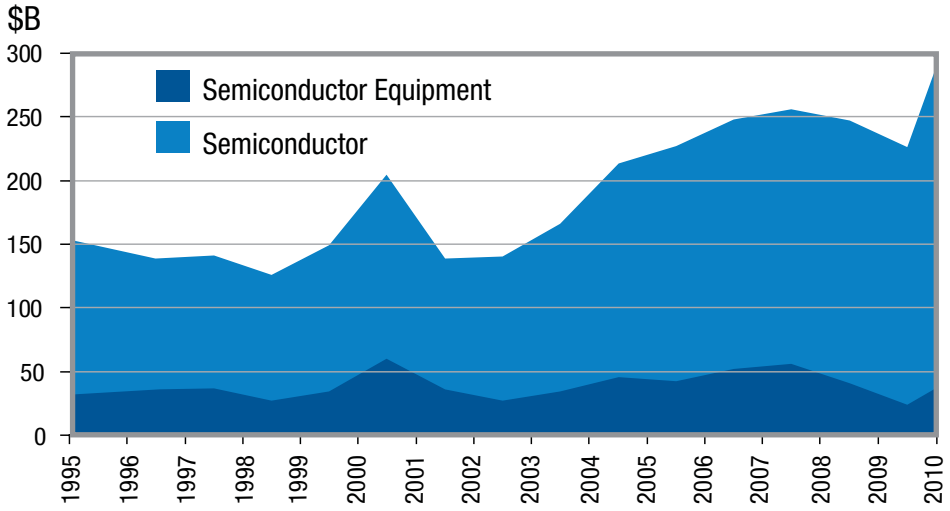
Setting New Directions for Our Industry

Semiconductor revenue and CAGR trends



Semiconductor CAGR	
1984 – 2000	11.6%
2001 – 2009	5.6%
1984 – 1995	14.4%
1996 – 2009	3.4%

Equipment semiconductor CAGR	
1984 – 2000	15.3%
2001 – 2009	-5.9%
1984 – 1995	16.0%
1996 – 2009	-3.6%

Source: VLSI Research Inc.

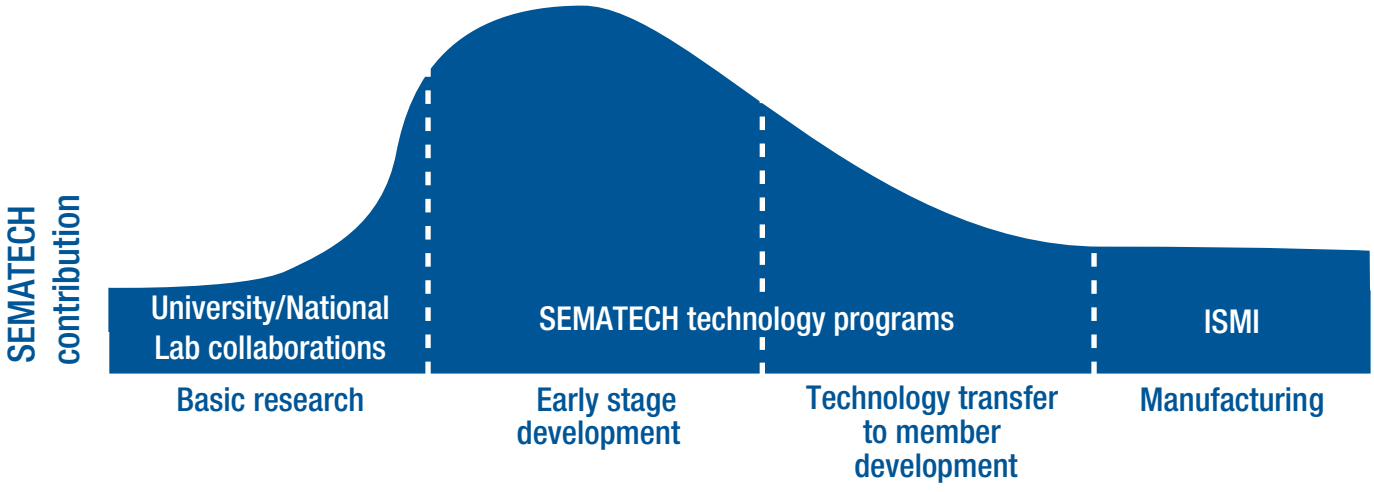
Strong partnerships create a foundation for growth

Worldwide comprehensive industry collaboration is critical to resolving the R&D funding gap and ensuring the health of the industry—and individual companies—for years to come. SEMATECH's strong partnerships with universities, national laboratories, semiconductor companies, equipment and materials manufacturers, regional governments, other consortia and industry experts from around the world have enabled us to keep the industry on track to realize the Roadmap.

While much collaboration already exists within the industry, a different mode of collaboration is now required. To continue to develop a technology pipeline that complements the current infrastructure and comprehends changing business models, a much broader and deeper industrial collaboration is needed more than ever before, extending to the systems, design, fabless, test, assembly and packaging communities.

The benefits of such partnerships are clear: working together, semiconductor R&D organizations can achieve better leverage, more efficiency, and faster execution.

SEMATECH role



The Power of Collaboration

Setting New Directions for Our Industry

A collaborative ecosystem

When it comes to research and development solutions for semiconductor and equipment manufacturers, SEMATECH plays a pivotal role in laying the foundation for some of the industry's greatest breakthroughs and the transition to next-generation technologies—all to better serve our members. At SEMATECH, we value:

Collaboration—we address complex industry-wide challenges through collaboration across disciplines, institutions and perspectives around the globe.

Innovation—we are committed to developing cutting-edge technology, driving manufacturing productivity, leading industry-wide initiatives and establishing industry infrastructure and standards.

Members—we recognize strength in the diverse participation in consortium activities, with a flexible approach to engaging members and conducting programs that align with greater industry needs and enable major industry transitions.

Knowledge—we share a passion for knowledge and encourage the exchange of information through the SEMATECH Knowledge Series, a variety of public industry workshops, meetings and events held throughout the year.

Excellence—we aspire to excellence, innovation and relevance in all that we do.

> *"EUV mask defectivity is the single greatest challenge to EUV readiness, but finding the defects requires metrology tools that do not yet exist. These tools will not be available in time without intervention, and the industry agrees that SEMATECH is the place to come together and partner for solutions."*
>
> **—John Warlaumont,** Vice President of Advanced Technology, SEMATECH

New initiatives to address key industry needs

SEMATECH drives world-class R&D in critical areas of advanced technology—lithography, new materials and device structures, and metrology—exploring ways to extend current technologies while building the infrastructure for emerging next-generation technologies.

As industry leaders in the development of manufacturable and cost-effective solutions for semiconductor applications, SEMATECH scientists and engineers conduct extensive R&D across a broad program portfolio.

Our goal is to foster innovation and deliver real world results that allow our members to make strategic decisions on novel processes, tools and materials and to accelerate their time to market.

Driving innovation and enabling transformation across the entire semiconductor ecosystem

This year, more than any other, SEMATECH focused on leading the industry in addressing key infrastructure gaps, providing a single voice to the industry in areas such as standards, leveraging resources and technical knowledge throughout the industry, and working on early materials efforts to reduce the number of potential options.

In the capital-intensive semiconductor industry, cost-of-ownership issues are critical to the bottom line. SEMATECH focuses on cost of ownership by working to extend current technologies to their limits while at the same time preparing for transitions to next-generation technologies. SEMATECH is creating the partnerships required to build the capital-intensive extreme ultraviolet (EUV) lithography infrastructure by launching the EUV Mask Infrastructure (EMI) Partnership, an industry-wide collaboration consisting of major semiconductor manufacturers and mask and mask blank suppliers. The EMI plans to assure the development of EUV mask metrology tools including an aerial image tool for defect review (AIMS), an actinic blank inspection tool (ABI), and an advanced patterned mask inspection (PMI) tool. In 2010, the AIMS tool supplier was selected and development begun. The magnitude of the EMI program is already over $100 million and may approach $200 million when all tool programs have been selected and negotiated.

Similarly, SEMATECH is building critical industry infrastructure to drive 3D into mainstream high-volume manufacturing (HVM) by teaming with the Semiconductor Industry Association (SIA) and Semiconductor Research Corporation (SRC) to establish a new 3D Enablement Center to drive cohesive industry standardization efforts and technical specifications for heterogeneous 3D integration. The program aims to establish the infrastructure necessary for the industry to leverage 3D packaging technology for innovative new applications. Addressing these industry infrastructure gaps in phases, the primary focus of the

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3D Enablement Center will be on developing the requisite standards and technical specifications, followed by planning activities to identify the key areas for developing design tools to support 3D chip design.

The industry is characterized by a rapidly changing structure and an elaborate value chain. As the industry evolves, new players are entering the market and increased competition is prompting companies to anticipate and respond quickly to ever-changing customer demands. To address evolving business models, increasing industry segmentation, and diverging technology differentiation, SEMATECH created a new strategic initiative in 2010 to broaden the scope of our member participation and expand our program portfolio to the fabless community. By expanding our membership in this way, SEMATECH has gained valuable insights from the design community on implementation requirements for technologies such as 3D interconnects, next-generation lithography and novel materials and structures.

In June 2010, the campaign to recruit members from the fabless sector proved successful with the announcement of Qualcomm joining as SEMATECH's first integrated fabless chip manufacturer. Qualcomm's high-level engagement will assess the feasibility of technologies that are designed to extend Moore's Law.

In another effort to expand our R&D portfolio, SEMATECH investigated a variety of emerging materials and devices beyond CMOS that promise to revolutionize information technologies. These technologies, including high-k/metal gate, III-V materials, resistive RAM, carbon nanotubes and semiconductor nanowires as high-mobility materials for future high-speed and low-power transistor applications and interconnect applications, are expected to provide an evolutionary path to the 22 nm node and beyond. During 2010, SEMATECH made several breakthroughs in developing solutions for new high-mobility channel materials and devices, FinFETs and nanowire devices, emerging memory devices, and technologies beyond CMOS devices in the "More than Moore" space. These efforts aim not only to extend incumbent technologies, but also to enable future low- and ultra-low power devices, which are increasingly important for mobile as well as cloud computing systems.

"The semiconductor industry, specifically the development of 3D integration, is at an inflection point. In tackling the challenges faced by lack of standardization, we will have deep collaboration with SEMATECH and SRC addressing both bonding processes and 3D inspection. The program will accelerate the adoption of 3D integration technology."

—John E. Kelly III, Senior Vice President and Director of Research at IBM, and Chair SIA's Technology Steering Committee

"SEMATECH's leadership and innovative thinking in new materials, processes and concepts will enable CMOS scaling and pave the way for emerging technologies."

—Raj Jammy, Vice President of Emerging Technologies, SEMATECH

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Setting New Directions for Our Industry

Collaborative partnerships—a vehicle for co-creation

Complex issues call for complex solutions. No one entity can do it alone. SEMATECH fosters cooperation among diverse industry sectors by forming collaborative partnerships with key constituents and, in turn, helping the industry address many of its R&D challenges, avoid costly research dead-ends, eliminate redundant efforts and cut costs by sharing resources.

Besides our technical expertise, SEMATECH is best known for working closely with research partners to identify discoveries and approaches that can be pulled into the commercialization pipeline. With over 60 university collaborations across the world, SEMATECH has access to experts in many disciplines, as well as outstanding laboratories and development fabs to help test and perfect innovations and new applications. With an eye toward manufacturability and affordability, our work ranges from testing for feasibility to refining new concepts, techniques, tools, and materials.

In our cornerstone alliance with the College of Nanoscale Science and Engineering (CNSE) at the University at Albany—SUNY, SEMATECH has played an integral role in establishing upstate New York as a global semiconductor and nanotech cluster. This "Tech Valley" corridor currently has over $13 billion invested in technology-related programs and facilities, either by corporations or local and regional educational and technical training institutions that graduate thousands of highly skilled workers each year. Leading-edge innovation in nanotechnology and manufacturing is contributing to a growing global presence in the region; in fact, over 250 companies now operate in the area. SEMATECH's presence will continue to support the dramatic acceleration of the economic expansion in the region.

> *"SEMATECH's strong affiliation with chip manufacturers and suppliers, universities and research institutions around the world, coupled with its R&D capabilities and technical knowledge, offers an excellent opportunity to enhance our participation in the industry's technology agenda and help shape the industry's direction."*
>
> **—Jim Clifford,** Senior Vice President and General Manager, Qualcomm CDMA Technologies

In September 2010, Governor David A. Paterson and Assembly Speaker Sheldon Silver joined SEMATECH President and CEO Daniel Armbrust and CNSE Senior Vice President and CEO Dr. Alain Kaloyeros to announce the transition and expansion of the International SEMATECH Manufacturing Initiative, Inc. (ISMI), a subsidiary of SEMATECH. Beginning in January 2011, ISMI will partner with CNSE on advanced manufacturing technologies that are critical to enabling the fabrication of multi-functional computer nanochips, which drive nearly every facet of society, from the electronics, information technology, automotive and military sectors to emerging opportunities in clean energy and health care, among many others.

ISMI's programs—which range from pioneering work in conserving resources and reducing the industry's environmental footprint, to paving the way for the next transformational shift to 450 mm wafers in semiconductor manufacturing—are leading the industry forward in integrating technology innovations with manufacturing best practices to accelerate the commercialization of chips that enrich our daily lives.

The strategic alliance of SEMATECH and CNSE, now to be joined by ISMI, is making significant contributions to advancing state-of-the-art semiconductor manufacturing and next-generation microprocessors. It also reinforces the synergies that are part of the "clustering" economic strategy for New York's Capital Region.

ISMI holds a unique place in our industry as the only consortium focused on manufacturing, rather than R&D. Our members collaborate on ways to improve manufacturing productivity and reduce costs in today's manufacturing facilities and future factories.

ISMI has accomplished groundbreaking work in preparing for a cost-effective 450 mm transition, including projects to address the readiness of silicon, equipment and factory infrastructure. The next step will be more intensive work with equipment manufacturers to increase the supply of 450 mm wafers, generate 450 mm test wafers and demonstrate 450 mm equipment capabilities, and subsidize capital requirements. In 2010, the 450 mm program made significant progress in early design/prototypes, carrier/loadport interoperability, test wafer generation, equipment performance metrics, and metrology and process equipment development and demonstrations.

To stay competitive, mature fab companies must drive innovation in manufacturing efficiency, constantly improving cost and productivity and extending the life cycle of equipment and fabs over many years and many technology generations. Continuous cost, productivity and

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sustainability pressures include aging equipment with limited original equipment manufacturer support, as well as limited industry leverage and competitor insight.

ISMI is addressing these challenges and improving manufacturing productivity, cost, and cycle time for a targeted segment of manufacturers with the launch of its new Mature Technology Fabs program in November 2010. The new program addresses the challenges faced by semiconductor companies with mature fabs, including cost and productivity issues, equipment lifecycle management, safety procedures and logistics.

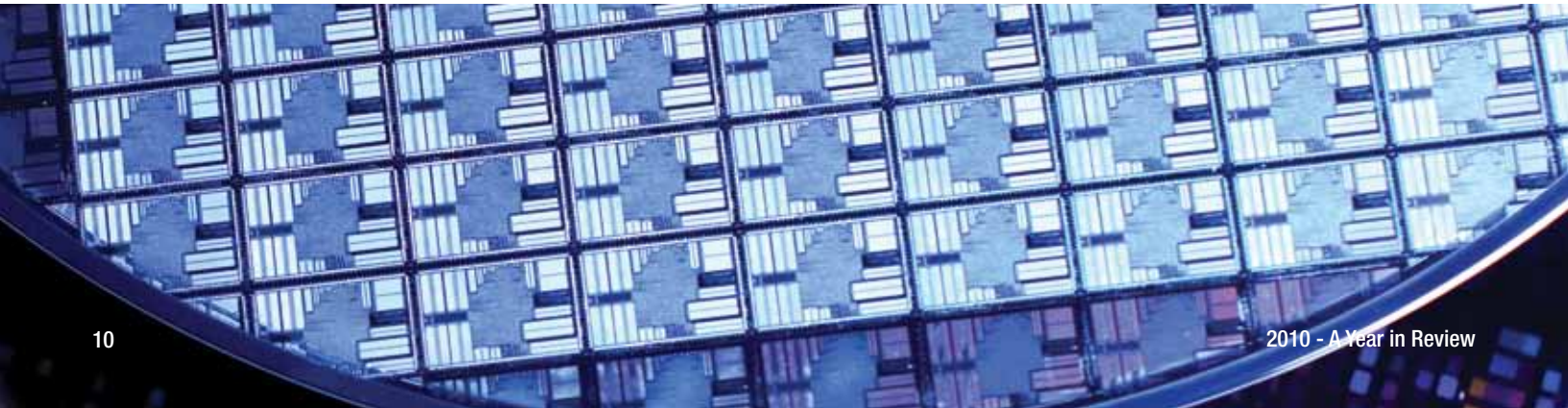
Formed in 2009, ISMI's Environment, Safety, and Health (ESH) Technology Center is working through all levels of the supply chain to address the industry's need for sustainability, productivity and cost-effectiveness. During 2010, Applied Materials and Edwards Limited joined the ESH Technology Center in cooperation with hundreds of ESH experts and consultants from around the world to develop data-driven solutions in energy and resource conservation, chemical management, and industry response to climate change.

"Industry collaboration is critical for staying on top of innovation in manufacturing. Our diverse knowledge will provide solutions that will allow IC makers with mature technology fabs to ensure profitability and competitiveness."

—Scott Kramer, Vice President of Manufacturing Technology, SEMATECH

"Using technological innovation, action and commitment, we can work together to find solutions to improving the environmental performance of our products and processes."

—Bruce Klafter, senior director for EHS and Sustainability, Applied Materials.



Increasing Participation and Membership

Throughout the year SEMATECH expanded its membership by adding new program members, representing major fabless companies and manufacturers of semiconductor equipment and materials. These new members enhanced the world-class capabilities and the roster of leading global companies at SEMATECH and enabled advanced technology solutions that are critical to the nanoelectronics industry.

February

Collaborating to address global environmentally sustainable and cost-effective manufacturing

Applied Materials joined other leading semiconductor manufacturers in cooperative projects for sustainable manufacturing as a part of ISMI's award-winning ESH Technology Center.

Advancing the development of next-generation patterning technologies

Dow Electronic Materials joined SEMATECH's Resist Materials and Development Center (RMDC) to collaborate with SEMATECH researchers at CNSE's Albany NanoTech Complex to develop and demonstrate extreme ultra-violet lithography (EUVL) materials and resists for use at the 22 nm node and beyond.

Collaborating to accelerate mask, source, and manufacturing solutions

ASML, a leading provider of lithography systems for the chip industry, and Tokyo Electron Limited (TEL) joined SEMATECH's Lithography program at CNSE's Albany NanoTech Complex. ASML teamed with researchers at SEMATECH to advance EUVL technology and its associated infrastructure components, including mask defect reduction, mask metrology infrastructure, source development, resist and materials development, and overall manufacturability and extendibility.

TEL is working alongside SEMATECH engineers to advance EUVL and related infrastructure, including mask defect reduction, mask metrology, source, resist processing, etch, and the overall manufacturability and extensibility of the technology.

May

Partnering to provide cost-effective semiconductor materials for the 22 nm node and beyond

JSR Corporation, an advanced materials supplier to chip-makers and others, its U.S. operation, JSR Micro, Inc., and AZ Materials, the global supplier of electronic materials to the semiconductor and flat panel display industries, became the newest members of SEMATECH's RMDC. These leading companies are collaborating with SEMATECH on key resist issues in EUV lithography including reduction or elimination of line edge roughness in lithographic images below 22 nm, ultimate resolution of newly formulated photoresists and testing of various imaging materials for EUV sensitivity.

June

Collaborating to broaden industry alignment on key roadmap challenges

Qualcomm Incorporated, a leading developer and innovator of advanced wireless technologies, products, and services, entered into a collaborative agreement with SEMATECH to advance CMOS scaling and assess new technologies. As the first integrated, fabless chip manufacturer to join SEMATECH, Qualcomm is participating in a high-level engagement to assess the feasibility of technologies that are designed to extend Moore's Law.

Partnerships to advance green semiconductor operations and processes for sustainable semiconductor manufacturing

Edwards Limited, a leading global supplier of vacuum and abatement equipment and services, joined ISMI's ESH Technology Center. Edwards is collaborating with ESH experts and consultants from around the world in the ESH Technology Center to develop data-driven solutions in energy and resource conservation, chemical management and climate change.

Partnering to develop TSV solutions for chip stacking

Lasertec Corporation of Japan joined SEMATECH's 3D Interconnect program to develop robust, cost-effective process metrology technology solutions for readying high-volume via-mid through-silicon via (TSV) manufacturing.

August

Collaborating to speed commercialization of mask lithography for semiconductor manufacturing

Dai Nippon Printing Co., Ltd. (DNP), a leading producer of semiconductor photomasks, and SEMATECH partnered to collaborate on methods for improving mask cleaning processes to reduce overall mask cost of ownership and accelerate commercial manufacturing readiness.

December

Partnering to extend the roadmap for non-volatile memory based on advanced material technology

Nanosys, Inc., an advanced materials architect, joined SEMATECH's Front End Processes (FEP) program. Leveraging SEMATECH's activities in advanced process integration and materials and device characterization, Nanosys and experts from our FEP research team are working to extend non-volatile memory for the 2X nm node and beyond. Specifically, SEMATECH and Nanosys will build a material and process infrastructure to enable and extend both planar and future 3D non-volatile memory technologies.

Global Industry Interaction

In 2010, SEMATECH sponsored our popular Knowledge Series, content-laden public conferences aimed at forging consensus and driving solutions to critical industry challenges. We delivered several hundred papers internationally and continued our instrumental support of the ITRS. No other industry engenders this kind of collaboration and interdependence, and SEMATECH is proud to play a leadership role in fostering creative cooperation.

Showcasing trends and leading technologies in lithography

Litho Forum
New York, NY; May

SEMATECH's biennial Litho Forum provides an opportunity for lithography users and suppliers to evaluate the progress of various technology options. The previous forums helped coordinate industry consensus for the 32 nm half-pitch generation and beyond.

The 2010 Forum attracted more than 200 technologists and executives from around the world. An impressive lineup of ranking leaders and technical experts in the semiconductor industry shared their perspectives on why collaboration is imperative for semiconductor innovation and what challenges the development of next-generation lithography technologies will face. Over 130 surveyed participants judged EUV to be the most likely candidate to be placed into manufacturing in 2014, with EUV extension being the technology of choice for 2016.

Maskless Lithography and Multi-beam Mask Writer Workshop
New York, NY; May

In conjunction with the Litho Forum, SEMATECH hosted a maskless and multi-beam workshop to review technical and business aspects of maskless and multi-beam technologies in relation to direct wafer imaging and as a solution for high speed mask writers. Co-sponsored by TSMC and Leti, the workshop facilitated discussion among 70 lithography technologists, mask fabricators, equipment suppliers, and development and manufacturing managers on current status, plans, and timelines, and conducted a technical survey of the participants. The top three issues from the survey included:

Throughput—Beam current versus throughput trade-off

Beam calibration, verification, and inspection on wafer

Beam stability/reliability

SEMATECH's 7th Annual Mask Cleaning Workshop
Monterey, CA; September

Held in conjunction with the SPIE Photomask Technology (BACUS) Symposium, this year's workshop focused on EUV mask lifetime under the best cleaning process. Mask manufacturers will face new hurdles in dealing with sub-30 nm particle removal, critical dimension uniformity, EUV reflectivity, or damage to EUV materials (Ru capping layer, Ta-based absorber layer, and ARC layers). Appropriate transport, handling, and storage technologies for EUV patterned masks after cleaning were also addressed.

International Symposium on Extreme Ultraviolet Lithography
Kobe, Japan; October

As a part of our ongoing commitment to help mature the technology and infrastructure for EUV lithography, SEMATECH sponsored the EUV Lithography Symposium, where the world's lithography experts gathered to crystallize the challenges to enabling EUV in production. This year, the main challenges were identified as:

- The creation of defect-free EUV masks and the attendant inspection and review infrastructure.
- The development of high power (200 W) EUV sources to support affordable HVM EUV throughput.
- EUV resist that simultaneously meets the resolution, sensitivity and line-width roughness (LWR) required by 22 nm production specifications.

International Symposium on Lithography Extensions
Kobe, Japan; October

Co-located with the EUV Lithography Symposium, this year's Lithography Extensions Symposium focused on efforts to extend 193 nm lithography to beyond the 22 nm half-pitch node. During the symposium, lithography technologists and engineers described progress on 193 nm high-index immersion lithography and other extensions to optical lithography and discussed emerging critical issues.

Global Industry Interaction

SEMATECH's Workshop on Directed Self-Assembly (DSA)
Kobe, Japan; October

DSA is a technology that combines lithographically defined features to guide self-assembled polymers by physical or chemical properties to create features smaller than those possible with optical lithography. Held in conjunction with Lithography Extensions Symposium, the DSA Workshop featured a series of presentations by experts in device design, lithography, and semiconductor processing on the potential application of DSA to semiconductor manufacturing as a candidate to extend optical lithography. Topics included:

- The proposed application of DSA to semiconductor manufacturing
- DSA applications that are a transition from current semiconductor manufacturing techniques to DSA methods
- Identification of early adopter opportunities
- Development results documenting DSA integration methods and characterization

Sharing knowledge on semiconductor manufacturing best practices and concepts

ISMI Installed-base Equipment Series

Throughout 2010, ISMI hosted a series of equipment productivity forums for IC manufacturers and original equipment manufacturers (OEMs). During these workshops, participants discussed key productivity and cost issues and focused on specific wafer fabrication equipment types. In addition, selected experts were invited to present their unique perspectives on topics related to the various tool types.

- Implant Equipment Workshop—Boston, MA; April
- Thermal Equipment Workshop—Austin, TX; March
- CVD Equipment Workshop—San Jose, CA; June
- Etch Equipment Workshop—San Francisco, CA; July
- Photo Equipment Workshop—Tokyo, Japan; September
- Wet Processing Equipment Workshop—Austin, TX, September
- Metrology Equipment Workshop—San Jose, CA; September
- PVD Equipment Workshop—San Jose, CA; October
- CMP Equipment Workshop—San Jose, CA; November

ISMI Manufacturing Week
Austin, TX; October

As the industry's most informative public exposition of manufacturing data, methods, and productivity boosters, the 2010 Manufacturing Week included the ISMI AEC/APC Symposium North America for the first time.

Highlights of Manufacturing Week included:

- AEC/APC sessions on data management and process control as well as equipment and process fault detection, classification, and control
- An interactive ESH session during which the audience identified and ranked critical issues that were then analyzed by an expert panel of industry leaders
- Updates on ISMI's Next Generation Factory and 450 mm Wafer Transition programs
- Papers offering "golden nuggets" of productivity and cost-cutting methods that can readily be applied to fabs of various sizes

Similar ISMI Manufacturing Week, events took place in Taiwan and Japan in conjunction with the SEMATECH Symposia.

Advancing new III-V semiconductor materials for volume wafer manufacturing

Surface Preparation and Cleaning Conference (SPCC)
Austin TX; March

For more than 10 years, SEMATECH's SPCC has brought together leading researchers from industry and academia to focus on challenges in advanced wafer and mask cleaning and surface preparation. Discussions during this year's conference focused on particle removal, including next-generation materials, controlling processes to minimize impact on fragile device structures, non-damaging methods to remove resist, and new metrology approaches for measuring passivation and surface defects.

Improving 3D interconnect processes

Stress Management for 3D ICs using Through Silicon Vias

These three one-day workshops, which attracted more than 150 technology managers from 78 companies and institutions in the U.S., Asia, and Europe, evaluated a design-for-manufacturing (DFM) approach to managing stress in 3D interconnects and driving consensus and support for these techniques across the industry.

- Albany, NY; March
- San Francisco, CA; July

Global Industry Interaction

SEMATECH's 3D Metrology Workshop
San Francisco, CA; July

Equipment suppliers shared their plans on how new and existing wafer metrology technologies can be used, modified or enhanced to measure and improve 3D interconnect processes.

Identifying strategies for advanced logic and memory technologies

The 7th Annual International Symposium on Advanced Gate Stack Technology
Albany, NY; September

More than 100 international researchers from industry and academia shared recent discoveries and outlined new gate stack strategies including high-k/metal gate stacks for silicon, silicon germanium, III-V high performance MOSFETs, and metal/high-k/metal stacks for resistance change memory, flash memory, and phase change memory.

Exchanging information and perspectives with colleagues around the world

SEMATECH Symposia

As part of our global outreach, SEMATECH hosted three symposia in Asia designed especially for regional semiconductor communities, including device manufacturers, equipment and materials suppliers, and university researchers. Attended by several hundred participants, these events featured keynote speakers, and interactive technical workshop sessions on critical areas of advanced and emerging technologies and manufacturing, such as EUV, 3D, advanced CMOS devices, emerging technologies, 450 mm, and manufacturing productivity, as well as a series of ISMI manufacturing-related workshops and councils.

- Hsinchu, Taiwan; September
- Tokyo, Japan; September
- Seoul, Korea; October

Technical conferences

In addition, throughout the year, our assignees and employees delivered more than 200 original papers, presentations, and joint reports in critical areas of advanced and emerging technologies.

- At the SPIE Advanced Lithography conferences in San Jose, CA, SEMATECH lithographers explored critical issues and potential solutions to preparing EUVL for high-volume manufacturing. SEMATECH papers featured advances in EUV resist development, including success with our 0.3 numerical aperture (NA) microexposure tools (METs) at CNSE and Lawrence Berkeley National Laboratory (LBNL). Other SEMATECH papers covered particle removal and inspection of EUV masks and metrology techniques for optical defect inspection and double patterning.
- With a focus on providing cost-effective and reliable solutions to accelerate the manufacturing readiness of 3D technology options, experts from SEMATECH's 3D interconnect program outlined new developments in wafer bonding, copper removal, and wafer thinning during the 2010 Materials Research Society (MRS) Spring Meeting in San Francisco, CA.
- At the International Symposium on VLSI Technology, System and Applications (VLSI-TSA), an international team of SEMATECH researchers reported on integrated approaches to CMOS logic and memory device technology and 3D TSVs.
- Attendees at the 2010 VLSI Technology Symposium listened to SEMATECH experts present the various ways SEMATECH is pursuing the power and performance features that are critical to implementing next-generation devices, based on leading-edge research in areas such as logic and memory technologies, high-k/metal gate materials, and non-planar and planar CMOS technologies including exciting new high-mobility channels and FinFET designs.
- To conserve energy resources and reduce costs of semiconductor manufacturing operations, ISMI's ESH experts reported on energy efficient strategies, addressing both fab facilities and processing equipment for semiconductor manufacturing operations at the International High Technology Environment, Safety and Health Conference (IHTESH) in Hsinchu, Taiwan.
- At the 56th annual IEEE International Electron Devices Meeting (IEDM) engineers from SEMATECH highlighted research breakthroughs on resistive RAM memory technologies, advanced fins and nanowire FETs for scaled CMOS devices, high-mobility III-V channel materials on 200 mm silicon wafers in an industry standard MOSFET flow, and future ultra-low power tunneling FET devices, emphasizing the growing need for higher performance and low-power devices.

Technical Programs

"At SEMATECH, research projects in advanced and emerging technologies span early-and late-stage research and development. As a leader in these fields, we partner with fellow experts at industrial, academic, and national laboratories to develop our technologies into commercially viable assets. This year, SEMATECH engineers realized major milestones in R&D programs that promise to advance the electronics industry."

—Dan Armbrust,
President and CEO, SEMATECH

3D Interconnect

Pushing the Third Dimension onto Moore's Scaling Path

The tremendous advantages of 3D integration—higher performance, increased functionality, lower cost and smaller chip size—have drawn considerable attention from a wide variety of companies across the semiconductor industry. Although 3D architectural concepts have been on the industry's radar for decades, adoption is now rapidly spreading, thanks to both the need for 3D and recent advances in stacking technologies. Worldwide academic and industrial research activities are currently focusing on developing new and improved technologies, and the stacked wide I/O DRAM for mobile applications promises to be the first high-volume manufacturing product to realize 3D's potential as a manufacturable and affordable path to sustaining semiconductor productivity growth.

Combining disparate technologies into a single chip

To build critical industry infrastructure and drive 3D into mainstream high-volume manufacturing (HVM), the industry still needs to come to a consensus on the most promising and cost-effective options.

At SEMATECH, our emphasis is on exploring 3D technology options that provide cost-effective and reliable solutions to drive the manufacturing readiness of 3D through-silicon vias (TSVs). One example is reducing the excess deposition of copper (or "overburden") while achieving void-free fill of 5x50 micron, 10:1 aspect ratio structures, for which the overburden thickness varies as a function of TSV geometry. In 2010, SEMATECH and its partners developed a practical approach to bottoms-up, void-free copper plating, that significantly reduced the copper overburden, allowing low-cost chemical mechanical polishing to be used instead of custom polishing slurries, in addition to achieving good planarization results, with low polish defects, at a rate suitable for emerging 3D TSV copper applications.

SEMATECH has assembled the combination of core technology know-how in wafer and die bonding, manufacturing infrastructure, and high volume experience, as well as a strong suite of process and metrology equipment to develop the building blocks required for 3D integration. Focusing on a via-mid approach, with copper-to-copper bonding covering both die-to-wafer and wafer-to-wafer integrations, SEMATECH has demonstrated 300 mm tooling, materials, and process module solutions necessary for 3D TSV manufacturing for 300 mm wafers in 2013 and beyond. In 2010, our efforts yielded progress toward the use of a common reference flow that would help drive consensus among the industry and lend validity to a cost model.

Despite its high potential, a lack of uniform standards and a limited understanding of key manufacturing parameters have so far prevented 3D technologies from being used in mainstream production. In December 2010, SEMATECH teamed with the SIA and SRC to establish a new 3D Enablement Center to build critical industry infrastructure and drive cohesive industry standardization efforts and technical specifications for heterogeneous 3D integration. Looking ahead to 2011, the program will focus on developing technologies and specifications necessary to establishing standards in critical areas such as inspection, metrology, microbumping, bonding, and thin wafer and die handling.

In an effort supported by the conventional CMOS processing capabilities in the 300 mm line at the College of Nanoscale Science and Engineering (CNSE) of the University at Albany, SEMATECH researchers are working jointly with chipmakers, equipment and materials suppliers, and universities on device interactions for fabrication at the 65 nm node for planar and future scaling to 30 nm for planar and non-planar CMOS technologies.

Taken together, SEMATECH's developments in TSVs, bonding, stacking, and thinning of test structures give us a strong foothold in this rapidly growing field. With recent investment in our facilities and our research capabilities, SEMATECH is well positioned to accelerate its work in 3D interconnects and help accelerate the adoption of this technology among our members and across the industry.

Distinctive technology capabilities

- Access to a fully integrated 300 mm R&D line at CNSE
- TSV interconnects
- Via-mid process flow
- 5 micron diameter, 50 micron deep TSVs
- Metallic (copper-to-copper) bonding
- Back-to-face and die-to-wafer bonding
- Robust pre-stacking, thinning process
- A common reference flow to build consensus on 3D IC technology options, standards and cost modeling

2010 key accomplishments

- Established an array of metrology techniques for characterizing a manufacturable wafer bond process to deliver a void- and dendrite-free bond for handle wafers.
- Acquired, installed and qualified the complete equipment set necessary for via-mid TSV technology.
- Characterized and hardened selected tools to ensure a robust equipment set for 3D TSV technology.
- Characterized and developed both wafer-to-wafer and die-to-wafer processing as well as associated metrology, including

3D Interconnect

a state-of-the-art wafer bonder from EVG, capable of copper-copper thermo compression, tack and fusion bonding; a wafer backgrind tool from Okamoto; a wet hood for chemical thinning and cleaning; and a TSV depth metrology tool from Lasertec.

- Evaluated micro-Raman spectroscopy in conjunction with finite element modeling in support of the die-to-wafer 5x50 micron reference flow.
- Demonstrated a die-to-wafer integration with 5x50 micron TSVs and copper-copper bonding.
- Delivered optimized processes for the TSV module (5x50 micron TSV RIE, liner/barrier/seed, Cu plating, and Cu CMP), handle wafer bonding, wafer thinning, TSV reveal from the backside, copper-copper thermo compression bonding, and backside metallization.
- Evaluated different metrology techniques for in-line TSV depth and profile measurements, including the suitability of different metrology techniques such as scanning acoustical microscopy (SAM) and infrared (IR) for implementation in HVM to assess bond quality.
- Hosted industry-wide workshops and forums to drive industry consensus by identifying critical infrastructure and technology gaps.

Sitaram Arkalgud
Director, Interconnect

Lithography

Extending the Pace of Semiconductor Innovation

Lithography is the primary enabling technology for semiconductor manufacturing. By providing the capability to continuously reduce the size of features patterned on semiconductor wafers, each new generation of lithography equipment has enabled faster microprocessors and smaller, less costly integrated circuits. Without the continuous improvements in lithography process and equipment technology that have occurred over the past 45 years, personal computers, cell phones and the Internet would not be available today.

However, current lithography techniques have been pushed about as far as they can go. Semiconductor manufacturers are at a critical juncture. Soon they must decide which lithographic horse to back in the race to the next generation of microchip manufacturing.

Building the infrastructure to enable low cost scaling

At SEMATECH, we focus on cost of ownership by working to extend current technologies as long as possible and by preparing for transitions to next-generation technology.

In 2010, more than any other year, SEMATECH focused on leading the industry in providing critical information and solutions for current and emerging lithography systems. Currently, extreme ultraviolet lithography (EUVL) is considered the most feasible alternative technology. However, it faces significant infrastructure challenges.

"A lithography technology will be introduced into manufacturing only if the entire supporting technology infrastructure is available."
—Dan Armbrust, President and CEO, SEMATECH

The greatest challenge is identifying committed suppliers to build small market EUV mask blank inspection hardware followed by at-wavelength imaging and patterned inspection hardware. With a total development cost estimated to be over $200 million, the only viable solution is to foster industry-wide financial support. In 2010, SEMATECH pursued the partnerships required to build the capital-intensive EUV infrastructure and in February, SEMATECH launched the EUV Mask Infrastructure (EMI) Partnership, a program that connects multiple segments of the EUV supply chain to collectively fund the development of needed metrology tools by equipment suppliers. The EMI's mission is to enable EUV mask tool solutions for a pilot line for process development by 2011 and full production capability by 2013.

Due to the cost and complexity of an EUV infrastructure, SEMATECH has established development centers in both EUV mask blank defect reduction and resist and related materials. SEMATECH's Mask Blank Development Center (MBDC) leads the industry in the defect reduction learning that is critical to achieving a defect-free mask blank supply for the introduction of EUV into high volume manufacturing EUV by 2013/14. The MBDC's 2010 experiment-driven exploration of the source of multilayer deposition adders resulted in reducing the average defects per blank in the best bin from 44 at the end of 2009 to 15 by the end of 2010. More importantly, the program accomplished this by developing world-class knowledge of very small defect compositional analysis using the Titan transmission electron microscope and installing an auger tool.

The Resist and Materials Development Center (RMDC) consists of the ASML alpha demo tool (ADT) currently at the University at Albany's College of Nanoscale Science and Engineering (CNSE), the Exitech microexposure tool (MET), and the Lawrence Berkeley National Laboratory MET. Additionally, the RMDC includes a large portfolio of resist research projects employing dozens of academic and industry researchers from around the world. For example, in 2009 the RMDC had three resist members; by the end of 2010, it had eight, encompassing almost the entire resist community. Together with its members, SEMATECH's RMDC provides the hardware and research expertise required by materials suppliers and member companies to develop EUV resist processes that meet the stringent resolution, linewidth roughness, and sensitivity specifications needed for EUV insertion at member companies.

Looking even farther into the future, SEMATECH will explore novel and potentially disruptive lithography technologies, such as nanoimprint and maskless direct write to evaluate their readiness and feasibility as emerging lithography solutions.

Distinctive technology capabilities

- EUV manufacturability and extendibility
- Mask infrastructure
- Resist/materials development
- Alternative lithography

2010 key accomplishments

Defect reduction

- Demonstrated a 60 percent reduction in the total defects on EUV mask blanks at a 30 percent process yield. This is a significant improvement in the rate of blank defect reduction. Over the past 12 months, EUV mask blank defects have been reduced from an average of 44 defects per mask blank to 18 defects per mask blank.
- Developed an iridium film deposition and etchback process that enables the analysis of non-conductive surfaces on the auger metrology tool. This process allowed, for the first time, auger analysis of defects on a non-conductive surface by creating a film thick enough to dissipate the surface charge but thin enough to allow the auger spectra to be obtained. This capability is critical to improving the overall quality of EUV mask substrates made of quartz and low thermal expansion materials.

Lithography

- Developed a low defect cleaning and film deposition process for the shields of the EUV mask blank deposition tool with the surface roughness required to reduce particle defects generated during the Si/Mo multilayer film deposition. This process eliminated 50 percent of the particle defects from the deposition and reduced by approximately 20 percent the remaining particles incorporated in the film.

Mask infrastructure

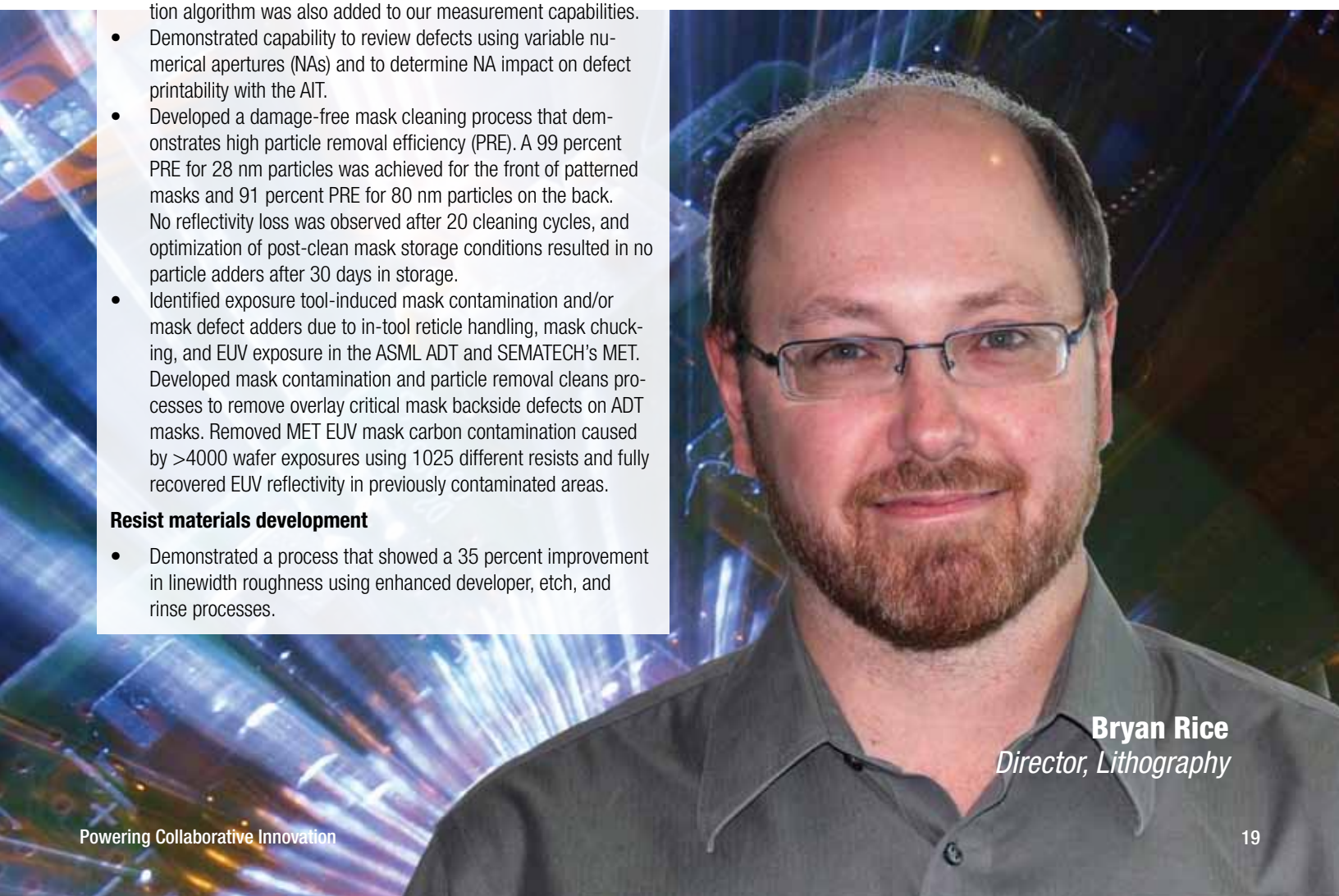
- Facilitated the capability of the latest generation mask pattern placement metrology tool being developed by SEMATECH's supplier partner to meet critical dimension reproducibility specifications on all structure sizes from 140 nm to 500 nm on the mask. Different illuminator settings were used to achieve these results. Short-term repeatability of 0.49 nm was demonstrated after corrections were made to the air flow to the optics and handler area.
- Demonstrated 65 nm line and space resolution with SEMATECH's aerial imaging tool (AIT). A new aerial image phase reconstruction algorithm was also added to our measurement capabilities.
- Demonstrated capability to review defects using variable numerical apertures (NAs) and to determine NA impact on defect printability with the AIT.
- Developed a damage-free mask cleaning process that demonstrates high particle removal efficiency (PRE). A 99 percent PRE for 28 nm particles was achieved for the front of patterned masks and 91 percent PRE for 80 nm particles on the back. No reflectivity loss was observed after 20 cleaning cycles, and optimization of post-clean mask storage conditions resulted in no particle adders after 30 days in storage.
- Identified exposure tool-induced mask contamination and/or mask defect adders due to in-tool reticle handling, mask chucking, and EUV exposure in the ASML ADT and SEMATECH's MET. Developed mask contamination and particle removal cleans processes to remove overlay critical mask backside defects on ADT masks. Removed MET EUV mask carbon contamination caused by >4000 wafer exposures using 1025 different resists and fully recovered EUV reflectivity in previously contaminated areas.

Resist materials development

- Demonstrated a process that showed a 35 percent improvement in linewidth roughness using enhanced developer, etch, and rinse processes.
- Imaged a record 9000 EUV resist wafers in the RMDC.
- Installed a dipole illumination capability that enables sub-20 nm resolution in the RMDC Albany MET.
- Demonstrated sub-14 nm resist modulation for a non-chemically amplified resist material with the RMDC Berkeley MET.
- Achieved a resolution of 25 nm with an improved resist process using the ADT.

Alternative lithography

- Demonstrated sub-15 nm overlay on 300 mm wafers using the nanoimprint tool.
- Printed high resolution 11 nm features using nanoimprint.
- Developed a 22 nm template with an array of customer designs including programmed defect structures, fresnel zone target, critical dimension small angle X-ray scattering targets, and dot structures that printed with 1 nm across-wafer critical dimension variation and 2.5 nm linewidth roughness.



Bryan Rice
Director, Lithography

Front End Processes

Accelerating the Next Transistor Revolution

Transistors have revolutionized electronics since they were first invented over half a century ago. Their importance today and their widespread success rest on our ability to mass produce them at the nanoscale using a highly automated process that achieves astonishingly low per-transistor costs. However, as transistor dimensions drop below 100 nm, the technology and design of conventional silicon-based CMOS processors are approaching their fundamental limits.

This rapid cadence of transistor scaling is helping the introduction of new technologies that are increasingly mobile, pervasive, and cost-effective—making life more productive. However, to handle the demands of the faster processing speeds and lower power consumption needed for such technologies, the industry must intensify research on scaling complementary metal-oxide semiconductor (CMOS) technologies. To this end, SEMATECH is exploring innovative materials and new transistor structures to address key aspects of transistor performance, power, and cost.

Silicon (Si) and Si-based materials have been the basic layers used in manufacturing CMOS transistors, but these staples can no longer meet the performance needs of modern chip technologies. To extend or replace these Si-based layers, SEMATECH's core technical teams are continually seeking and producing the most innovative material and process solutions. Techniques for extending high-k dielectrics, metal gates, ultra-shallow low-damage junctions, low-resistance silicide and germanide contact technologies are some examples. To advance new structures within transistors, we are focusing on innovative options such as high mobility channels, quantum well channel architectures, and multi-gate devices like FinFETs, nanowire FETs and tunneling FETs. Advanced memory technologies such as charge trap flash, resistive RAM, and other emerging memory technologies are also being explored. In addition to making breakthroughs with these cutting-edge innovations, technologies beyond CMOS devices in the "More than Moore" space are likewise being pursued.

New materials

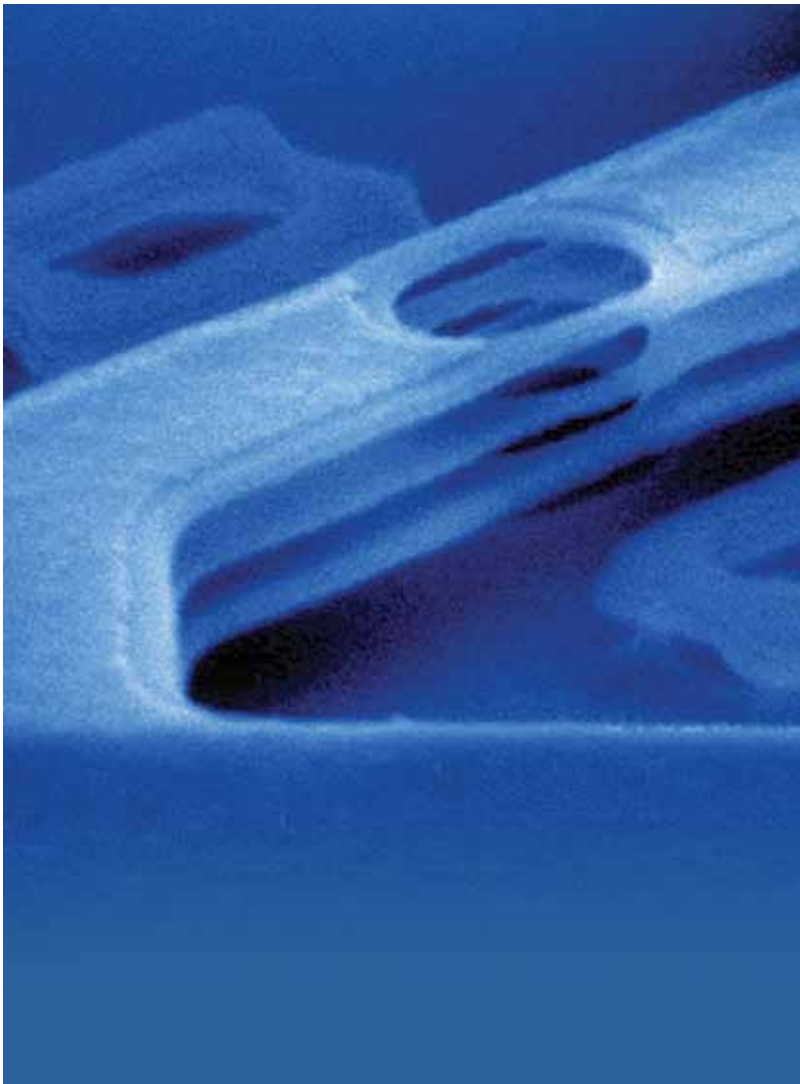
Although the materials used in CMOS devices have been slow to change, problems in chips can be addressed by adjusting the materials that compose them. New materials and material modifications include low-resistivity conductors, strained Si, high-k dielectrics in the front end, and low-k dielectrics in the back end.

To avoid further downscaling of CMOS technology, SEMATECH researchers are exploring ways to integrate new materials into Si channels, such as silicon-germanium (SiGe) and III-V that are applicable for the 16 nm node and beyond. A significant part of this effort is focused on developing low-defect density epitaxial Ge/III-V layers on Si and suitable techniques to form high quality high-k gate stacks, low contact resistance silicides through barrier height engineering, and low-damage ultra-shallow junctions.

Also being investigated is a non-planar device centered on high mobility FinFETs and nanowire FETs that can provide better electrostatic control and scalability than current planar device architectures. Crystal orientation and quantum well architectures are being evaluated to further the advantages of such devices. Novel materials and structures to address the aggressive scaling of flash memory technologies, as well as emerging memories like resistive RAMs, are likewise being explored.

Such alternative materials could potentially improve performance, but efficiently incorporating these new materials into existing device structures and manufacturing processes remains a challenge.

In 2010, we conducted several key R&D projects, including aggressively scaled (to 0.5 nm equivalent oxide thickness) high-k gate



Front End Processes

dielectrics on Si, appropriate metal gates (electrodes) for threshold voltage control in low-standby power and high-performance applications, high mobility channels using Ge-based and III-V based materials, non-planar transistor structures, advanced non-volatile memory devices and associated materials, and characterization and device models.

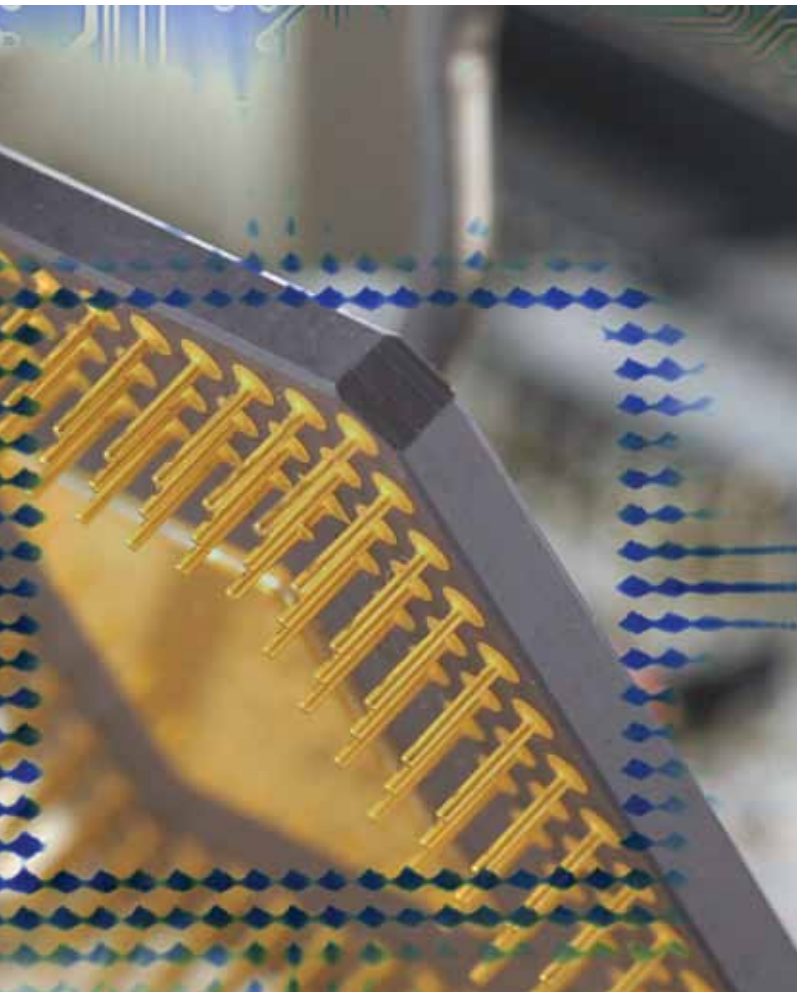
SEMATECH is also extensively involved in developing novel electrical/physical characterization methods to reveal the fundamental nature of the various materials used in device fabrication and the interactions among them. In collaboration with our member companies, the Semiconductor Research Corporation (SRC), leading universities and national labs, our group ensures that needed methods and models are developed and drives for common benchmarking standards to accelerate learning and commercial adoption. Efforts are underway to better understand the nature of defects in the various layers that dictate the final device behavior and reliability. Working with member companies, equipment and materials suppliers, and other partners, SEMATECH also develops the infrastructure in materials, processes, and tools to enable the adoption of future effective scaling options, often shaping the direction of the *International Technology Roadmap for Semiconductors* (ITRS).

These efforts aim not only to extend incumbent technologies but also to enable future low- and ultra-low power devices, which are increasingly important for mobile and cloud computing systems. As these path-breaking solutions are developed, we stay focused on providing a strong foundation in understanding fundamental material properties, process options, integration choices, reliability impacts, costs and complexity trade-offs that drive the scaling of device technology and its adoption into high-volume manufacturing. To identify the optimum device structures needed for future generation devices, SEMATECH is developing models through simulation and experimental work.

In 2010, SEMATECH researchers concentrated on developing low- to ultra-low devices, multifunctional high temperature stable devices and

Paul Kirsch
Director, Front End Processes

Front End Processes



sensors, and analog/mixed signal discrete components that can be deployed in conjunction with CMOS devices on the same Si platform to enhance functionality. Such options are critical for the future system-on-chip designs that are on the roadmaps of many leading chip makers.

Distinctive technology capabilities

- Advanced dielectrics and electrodes
- Planar and non-planar CMOS scaling
- Advanced memory device scaling
- Electrical and physical characterization
- Emerging technologies

2010 key accomplishments

- Demonstrated significant reductions in Schottky barrier height and contact resistance, enabling the continued enhancement of device performance beyond the 45/32 nm technology node. Contact resistance in source/drain regions, which comes from a relatively high Schottky barrier between n-type doped Si and NiSi, is one of the most pressing concerns in advanced CMOS technology.
- Demonstrated novel doping and activation schemes to form defect-free ultra-shallow junctions with a low resistivity for Si and non-Si channels in planar and non-planar forms.
- For the first time ever, demonstrated highly scaled FinFETs with high mobility SiGe channels exhibiting excellent electrostatic and transport properties for continued scaling in non-planar architectures.
- Established a state-of-the-art baseline flow with high-k dielectrics and metal gates that allows fundamental work on scaling high-k metal gate equivalent oxide thickness and serves as a standard vehicle for all CMOS scaling. Given that high-k metal gates are in manufacturing today, any new process/material/device options for the future should be studied with a baseline flow that incorporates them.
- Established a 1T1R flow for studying advanced emerging memory devices, which will be further refined in 2011. Such a flow allows exploration of resistive RAM (ReRAM) materials, electrodes and combinations of stacks derived at dimensions of industrial relevance. In addition, this flow also helps to better understand the fundamentals that drive switching behavior, retention, endurance, microstructural transformations, and switching energy in

Front End Processes

such emerging memory devices. This simple yet robust flow can also shed light on the type of driver device that will be needed for dense resistive RAMs.

- Demonstrated the feasibility to fully integrate III-V on Si on 200 mm wafers and form highly scaled devices using standard fab Si processing tool sets. This is a significant achievement in preparation for developing the infrastructure for III-V VLSI processing in a Si line.
- Demonstrated the first Si-based tFET with low subthreshold swing (~42 mV/dec) and reasonable Ion (~50 micro-amp/micron).
- Developed and demonstrated an in-line metrology system based on vacuum ultraviolet spectroscopic reflectometry for characterizing ultra-thin layers in gate dielectric stacks and thin SiGe layers for substrate engineering. This platform will be able to provide the highly accurate characterization needed for in-line metrology of advanced logic and memory applications for future technology generations.
- Because conventional characterization techniques that work with Si substrates do not necessarily work with III-V substrates, developed a new physical technique, second harmonic generation, which has been shown to correlate nicely with electrical results.
- Developed a key new mask set with test structures focused upon a range of devices (FinFETs, nanowires, and resistive RAM, in addition to conventional planar devices), as well as those intentionally designed to allow a connection from design to integration to test and reliability.
- Developed a foundation for testing and analyzing reliability data for a range of devices. As new materials are introduced, the long-term behavior of devices, reliability in particular, are of concern.
- Established the capability to test for both low frequency noise (LFN) and related random telegraph signals. Results have led to a model (including the energy of physical relaxation of the bonds around a trap) that appears to explain several issues that earlier noise models could not address.
- For memory devices, focused upon ReRAM devices, concentrating on material sets that can be easily incorporated into manufacturing sites. Although more exotic materials have shown some promise in the literature, we have found that with creative integration techniques, excellent switching characteristics are possible with modified conventional materials. Over 25 material systems have been evaluated, resulting in a Pt-free electrode stack with a fab-friendly metal oxide switching layer. In addition, low reset currents—down to 10μA—have been achieved.

International SEMATECH Manufacturing Initiative

Maximizing Productivity from Lab to Fab

There is constant pressure to cut costs, improve quality, meet environmental and international standards and bring new and improved products to market faster, all in a larger, more competitive global playing field. As manufacturers struggle to keep pace with accelerating changes, the mission of the International SEMATECH Manufacturing Initiative (ISMI) is to work with semiconductor manufacturers to improve their productivity and cost performance has become more critical than ever.

Building on the success of SEMATECH's collaborative research model, ISMI has proven its value to manufacturers as a growing source of innovation built on a strategic framework of cross-company collaboration. During 2010, these companies worked cooperatively in programs focused on continuous improvement, 300 mm next-generation fabs, 450 mm wafers, metrology, and environment, safety, and health—seeking lower per-wafer and per-die costs through advances in equipment, processes, resources, fab design and manufacturing methods.

"Manufacturers must position themselves strategically to manage: continuous improvement, technology acceleration, supplier development, sustainability and opportunities in concert to compete long term." —Joe Draina, Director of Advanced Manufacturing Programs, ISMI

For ISMI, 2010 was a year to expand its capacity and capabilities to address critical manufacturing challenges.

ISMI's 450 mm program began shifting emphasis to supplier and equipment readiness, along with tool demonstrations, while our Next Generation Factory (NGF) program will develop global infrastructure to support improved factory cycle time and decreased manufacturing costs. The continuous improvement and councils teams maintained their focus on finding solutions for installed base productivity issues through a variety of benchmarking and methodology-sharing forums. Our Metrology program played a key industry role in advancing the metrology capabilities necessary for future technology nodes.

Additionally, ISMI's Environment, Health and Safety (ESH) Technology Center provided industry leadership in sustainability and green initiatives, with enhanced value through new members from our supplier community. Edwards Limited, a leading global supplier of vacuum and abatement equipment and services, joined the Technology Center, collaborating with hundreds of ESH experts and consultants from around the world to develop data-driven solutions in energy and resource conservation, chemical management and industry response to climate change.

Launched in November, ISMI's new Mature Fab program recognizes the challenges faced by semiconductor companies with mature fabs, including cost and productivity pressures, equipment lifecycle management, safety procedures and logistics. To stay competitive, mature fab companies must continuously tackle cost, productivity and sustainability issues, including aging equipment with limited original equipment manufacturer support, as well as limited industry leverage and competitor insight.

The Mature Fabs program provides a suite of forums, councils, and workshops that bring subject matter experts, device maker managers, and suppliers together to discuss common problems, and identify solutions covering all aspects of semiconductor manufacturing and business operations.

"The Mature Fabs program provides a unique offering of the most effective methods for member companies to access and implement, allowing them to further stretch their resources and attain optimal levels of performance." —Sanjay Rajguru, Director, Mature Fabs program, ISMI

Distinctive manufacturing capabilities

- Global benchmarking and best practices forums for continuous productivity improvement of fabs and equipment
- Innovative manufacturing capabilities to solve common productivity, cost, and cycle time challenges in both mature and advanced technology fabs and equipment
- Environment, safety, and health technologies to improve resource conservation and manufacturing sustainability
- Driver of industry momentum to realize a cost-effective 450 mm transition

2010 key accomplishments

450 mm transition

- Fostered supplier relationships to drive industry momentum to establish 450 mm readiness in synch with member companies' needs.
- Assessed test wafer requirements and scope for an industry transition.
- Provided updates to factory interface (FI) test plans and test FI components for conformance to guidelines.
- Demonstrated early wafer cleaning and film deposition capability to transition to 450 mm.

Continuous improvement

- Enabled solutions to productivity detractor issues within existing factories.
- Identified cost improvements through identification of alternative sources for spare parts and cost reduction best known methods (BKMs).
- Conducted equipment productivity forums workshops in conjunction with ISMI Installed-base Equipment Series that focused on productivity improvements.

International SEMATECH Manufacturing Initiative

Next generation factory

- Developed an Enhanced Equipment Quality Assurance (EEQA) Data usage software application that demonstrated the features and capabilities to properly track and monitor equipment functional performance. It was demonstrated at ISMI Manufacturing Week.
- Completed two Predictive Preventive Maintenance (PPM) pilot projects, each involving data from two different member company fabs on two different tools, with two different suppliers and two different universities. Developed a class on PPM for our members.
- Uploaded a Metadata Conformance Analyzer (MCA) for member companies and suppliers. The MCA checks OEM implementations for conformance to SEMI standards and ISMI guidelines.
- Developed and released an EDA equipment simulator at the 2nd freeze level for suppliers. They can use the simulator to confirm the readiness of their Interface A implementations.

Metrology

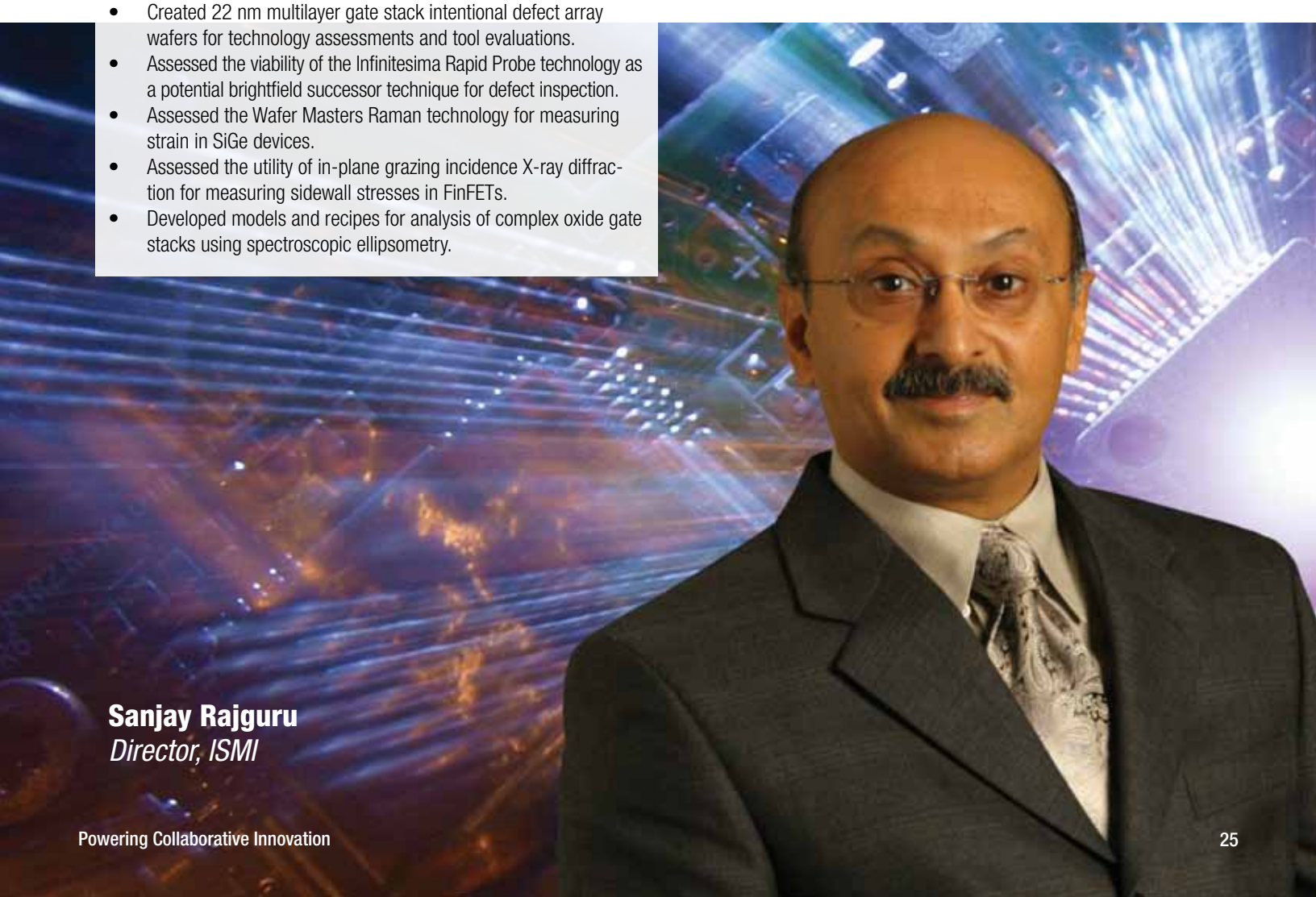
- Created 22 nm multilayer gate stack intentional defect array wafers for technology assessments and tool evaluations.
- Assessed the viability of the Infinitesima Rapid Probe technology as a potential brightfield successor technique for defect inspection.
- Assessed the Wafer Masters Raman technology for measuring strain in SiGe devices.
- Assessed the utility of in-plane grazing incidence X-ray diffraction for measuring sidewall stresses in FinFETs.
- Developed models and recipes for analysis of complex oxide gate stacks using spectroscopic ellipsometry.

Councils

- Provided and facilitated technical forums for semiconductor and manufacturing benchmarking and member sharing to drive world-class performance and cost.
- Conducted various workshops focusing in equipment productivity and factory improvement topics.
- Conducted meetings across councils to benchmark member company performance and provide sharing in the respective technology areas.

Environment, Safety, and Health Technology Center

- Enabled reduced consumption of semiconductor manufacturing resources, including energy, water, and chemicals.
- Provided ESH assessments of emerging technologies and processes.
- Provided technical support to address emerging global regulatory challenges and green initiatives.



Sanjay Rajguru
Director, ISMI

SEMATECH Executive Management

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President and Chief Executive Officer
(November 2009—present)

MICHAEL POLCARI
President and Chief Executive Officer
(January 2009—November 2009)

DAVID SAATHOFF
Senior Vice President and
Chief Administrative Officer

SCOTT KRAMER
Vice President of Manufacturing Technology

JOHN WARLAUMONT
Vice President of Advanced Technology

RAJ JAMMY
Vice President of Emerging Technologies

RANDY BARFIELD
Vice President of Finance and
Information Technology

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FULLER ROAD MANAGEMENT CORPORATION
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